An MMIC V-Band Phase-Locked Oscillator Using a GaAs MMIC Sampling Phase Detector

Atsushi Kanda, *Member, IEEE,* Tadao Nakagawa, *Member, IEEE,* Tetsuo Hirota, *Member, IEEE,* Hiroshi Okazaki, *Associate Member, IEEE,* and Masaru Nakamae

***Abstract*— A V-band full-monolithic phase-locked oscillator (PLO) has been developed. All the circuits are integrated into three monolithic microwave integrated circuit (MMIC) chips. One is a highly integrated multifunction MMIC for 15-GHz voltage-controlled oscillation and 15–30-GHz frequency doubling. The second is for 30–60-GHz frequency doubling. The third is a sampling phase detector (SPD) chip, which operates up to 20 GHz and can be driven at 0-dBm power. Each circuit is greatly reduced in size by using a uniplanar structure; the oscillator area is only 5.5 mm^2 and the SPD area is 3.0 mm^2. The PLO exhibits output power of 3.5 dBm with single-sideband (SSB) phase noise in the phase-locked state of -64 dBc/Hz at 10 kHz offset from 60.0 GHz in spite of the low Q full-monolithic oscillator circuitry.**

I. Introduction

THE LOCAL oscillator (LO) is the key device for frequency conversion in all microwave and millimeter-wave communication systems. Many systems need frequency synthesis for precise and fast frequency switching. As the demand for higher data transmission speeds increases, the RF will have to be increased, meaning millimeter-wave LO's will become more important. For the past few years, 60-GHz-band wireless communication experiments have been promoted by the Japanese government.

A very effective way to miniaturize communication equipment is to integrate RF components in monolithic microwave integrated circuit (MMIC) form. MMIC's are not used in many applications, however, because the combined cost of the chips and assembly make them expensive. Therefore, chip size should be reduced to lower chip cost and MMIC's should be integrated as highly as possible to reduce assembly costs. Higher integration will also prevent performance degradation caused by inter-chip connections.

Low phase noise and high stability are especially required for LO's in millimeter-wave communication systems. Coupling the oscillator with a dielectric resonator (DR) [1] is an easy way to reduce phase noise, but the oscillator could never be made smaller than the DR. Some reported millimeter-wave MMIC oscillators use a phase-locked loop (PLL) for stabilization [2], [3]. In a phase-locked oscillator (PLO), the oscillation frequency is divided or sampled in a feedback path and then compared with a reference signal. The frequency division scheme is used in most MMIC PLO's. But above the millimeter-wave region, the oscillation frequency is too high to be directly divided, and problems such as phase noise, spurs, and increased power consumption arise.

This paper describes the design and performance of a very compact V-band full-monolithic PLO that uses a GaAs MMIC sampling phase detector (SPD). Size is reduced by: 1) making maximum use of lumped-constant elements such as meander inductors, spiral inductors, and metal–insulator–metal (MIM) capacitors and 2) densely integrating the whole circuit using a uniplanar MMIC structure. The use of the compact MMIC SPD simplifies the PLO configuration and makes the phase noise of the PLO lower than that of PLL's using frequency dividers, which are now used in most MMIC PLO's.

II. Concept of Millimeter-Wave MMIC PLO's

A millimeter-wave oscillator can be achieved either by oscillation at a high fundamental frequency itself or by oscillation obtained from a low fundamental frequency oscillation by means of frequency multipliers. The former approach makes the oscillator smaller and simpler, but high-performance active devices such as high electron mobility transistors (HEMT's) or HBT's are needed for millimeter-wave oscillation. Moreover, a PLL cannot be used because of the speed limitation of the frequency dividers. In the latter approach, many phase-noise and spurious-signal-reduction techniques can be applied. Circuit scale tends to be large, however, because a large number of frequency multipliers are required to obtain the desired frequency. Thus, a high level of integration is important.

MMIC oscillators generally require an oscillation stabilizing technique because MMIC's have a poor quality factor Q. There are two effective ways to stabilize millimeter-wave oscillators: either the loaded Q (Q_L) of the oscillators can be increased by coupling them to high Q external DR's or a PLL can be used.

Adding high Q (unloaded Q, Q_u, is normally 1000–10 000) ceramic DR's is common in millimeter-wave oscillators. The oscillation frequency is determined by the material, the dimensions of the DR, and surrounding shields, while stability is determined by the coupling coefficient of the DR and circuit, which depends on the distance between them. Those dimensions and the coupling coefficient become critical for precise millimeter-wave oscillation as the wavelength becomes shorter. Therefore, a lot of attention must be given to the DR assembly processes, and this leads to poor yields and higher costs. Since the oscillation stability comes from the resonance,

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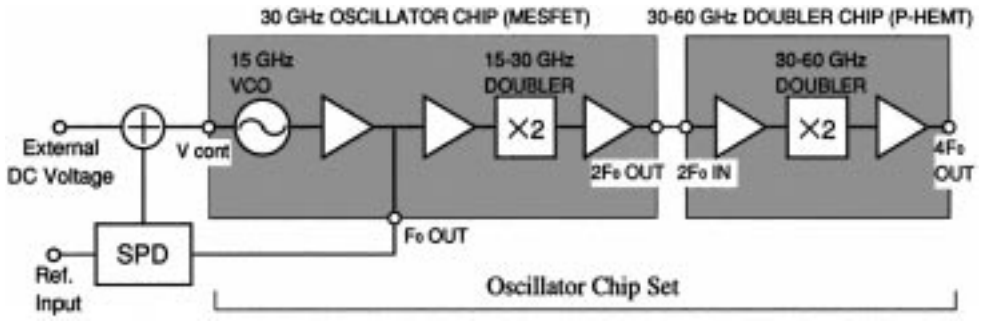
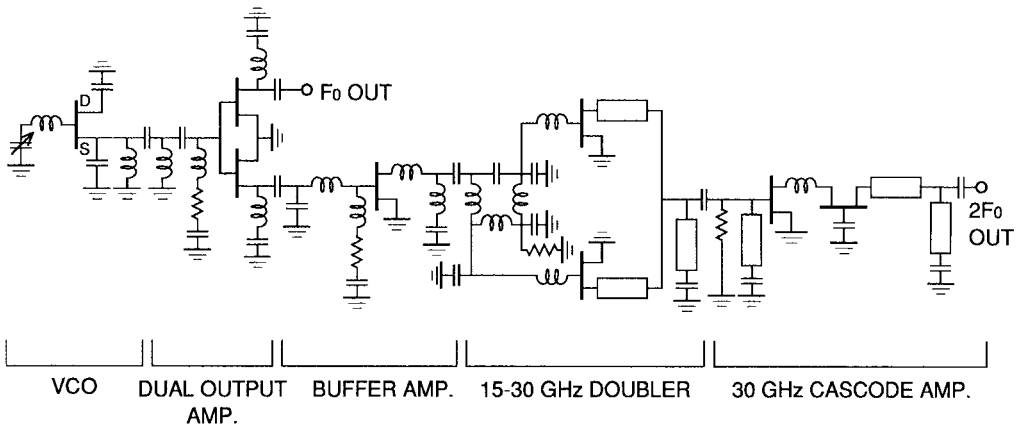
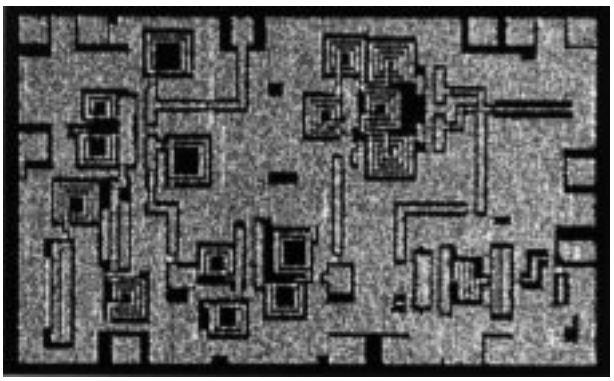


Fig. 1. A functional block diagram of the MMIC V-band PLO.



(a)



(b)

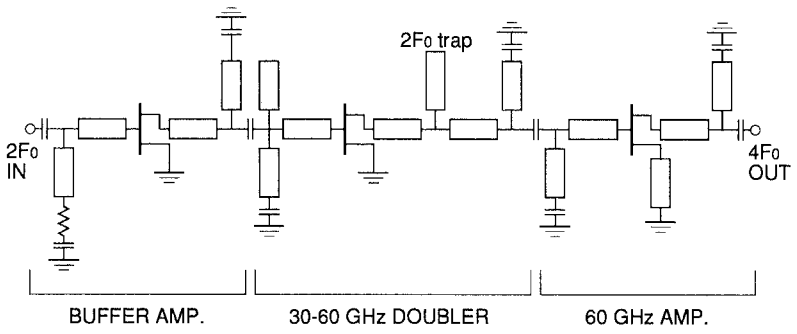
Fig. 2. (a) Circuit diagram. (b) Photograph of the 30-GHz oscillator chip.

DR's are used for fixed-frequency oscillators or for narrow-band oscillators even if the frequency is tunable. Therefore, DR oscillators (DRO's) in millimeter-wave communication are usually only used in LO's or in modulation sources in a single channel.

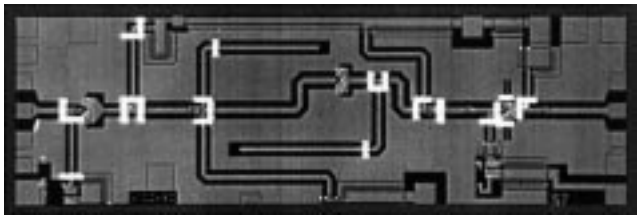
Using a PLL in millimeter-wave oscillators is not yet popular, but this approach is superior to adding DR's in that it provides long-term stability and reduces phase noise within the loop bandwidth. It also has the advantage of widening the frequency band.

PLL's can be categorized into two types: those that use a frequency division scheme and those that use a sampling phase detection scheme. MMIC PLO's with frequency dividers have been emphasized because it is easy to develop PLO's into synthesizers with programmable division ratios. In the millimeter-wave frequency range, however, even the fastest commercially available frequency dividers are not fast enough, so lower frequency PLO's must be used in conjunction with frequency multipliers. The larger the order of multiplication is, the larger the dimension of circuit becomes. In addition, the faster the frequency dividers operate, the more power they consume (of the order of several watts).

The SPD scheme has the potential to provide compact millimeter-wave MMIC PLO's with low phase noise and low power consumption without the use of any frequency dividers. But there has been some difficulty in developing MMIC SPD's because: 1) the step recovery diodes for the pulse generator cannot be fabricated using the GaAs MMIC



(a)



(b)

Fig. 3. (a) Circuit diagram. (b) Photograph of the 30–60-GHz doubler chip.

process and 2) the conventional SPD dissipates a lot of driving power. So the development of millimeter-wave MMIC PLO's has had to wait for the GaAs MMIC SPD to get over those weaknesses.

III. Configuration and MMIC Design

A block diagram of the MMIC PLO is shown in Fig. 1. It mainly consists of the oscillator chip set (two MMIC chips), the SPD circuit (one MMIC chip), and an external analog adder. A conventional signal generator was used for the PLL reference oscillator in the performance measurement.

A. The Oscillator Chip Set

The shaded areas in Fig 1. show the MMIC oscillator chip set [4]. The 30-GHz oscillator chip (see Fig. 2) was fabricated with a high-yield 0.3-μm self-aligned ion-implanted MESFET process [5]. The FET devices have a cutoff frequency (f_T) of 20 GHz, maximum oscillation frequency ($f_{\max}$) of 70 GHz, and dc transconductance (G_m) of 200 mS/mm. The chip includes a 15-GHz voltage-controlled oscillator (VCO), a 15–30-GHz balanced frequency doubler, and an output cascode amplifier [6]. The circuit area is only 2.2 $\times$ 1.3 mm^2, due to the maximal use of lumped-constant elements, i.e., meander inductors, spiral inductors, and MIM capacitors. The VCO employs a common drain configuration, a spiral inductor resonator. The frequency is tuned by a 240-μm gate-width FET working as a varactor diode. The output of the VCO is split by a dual-output amplifier [7]. One of the amplifier outputs is for the PLL and the other is fed to the frequency doubler. The two outputs are sufficiently isolated from each other owing to the isolation of the amplifier. The 600-μm-thick substrate does not need polishing for proper circuit operation due to the use of the uniplanar structure.

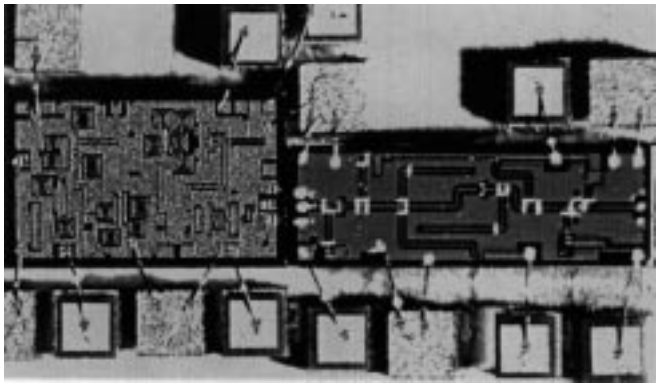


Fig. 4. Photograph of the oscillator chip set. The two chips are connected with Au wires. Chip sizes are 2.2 $\times$ 1.3 mm^2 and 2.9 $\times$ 0.9 mm^2.

The other chip, the 30–60-GHz doubler shown in Fig. 3, was fabricated with a 0.1-μm pseudomorphic (PM) low-noise AlGaAs/InGaAs/GaAs HEMT process. The PM HEMT devices have a cutoff frequency (f_T) higher than 70 GHz, maximum oscillation frequency ($f_{\max}$) higher than 110 GHz, and typical dc transconductance (G_m) of 400 mS/mm. The chip includes a buffer amplifier, a 30–60-GHz frequency doubler, and a 60-GHz amplifier. The wide use of coplanar waveguides reduces the circuit area to 2.9 $\times$ 0.9 mm^2. The buffer amplifier weakens the influence of significant changes in the input impedance of the frequency doubler. The frequency doubler has a single gate configuration and an open stub is used at the output of the PM HEMT to suppress the 30-GHz signal. The HP–Root model [8] was employed to optimize the nonlinear design of the frequency doubler. Precise device modeling and uniplanar element libraries yield a high conversion gain.

A photograph of the oscillator chip set as a unit is shown in Fig. 4. The two chips are connected by 20-μmϕ Au wires. The

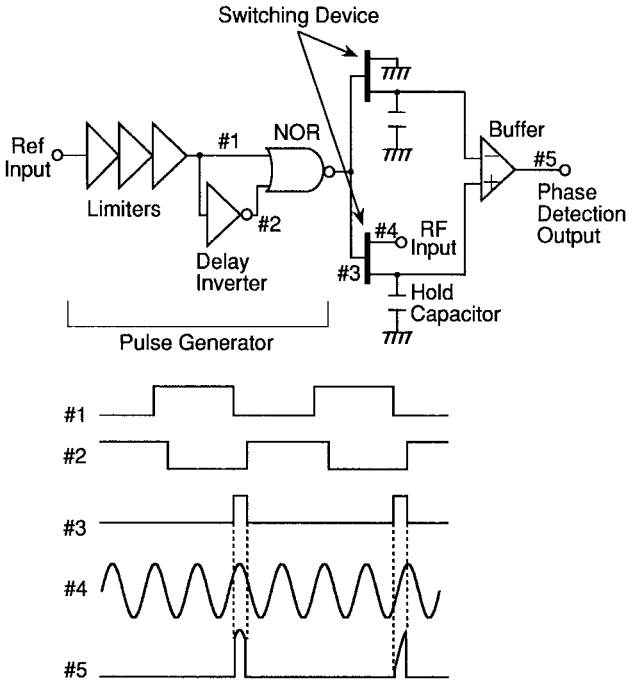


Fig. 5. Configuration and principle of the MMIC SPD.

uniplanar structure allows a high level of integration and thus reduces the chip size. Integration leads to a decrease in the number of wires. Moreover, the small chip size helps to avoid undesired parasitic resonance caused by the cavity around the IC in a package.

B. The SPD Circuit

The configuration and principles of the SPD are based on a previously reported MMIC SPD [9] and are shown in Fig. 5. The pulse generator consists of limiters, a delay inverter, and a NOR gate. The switching devices are transfer-gate FET's. Two FET's are arranged in a balanced-like configuration to suppress the leakage of the sampling pulses, which are canceled at the following buffer amplifier. The reference input sinusoidal wave is shaped into a square wave by the limiters. The wave is then split in two with one part going to the NOR gate directly and the other passing through the delay inverter. Thus, narrow pulses synchronized to the reference signal are obtained at the NOR gate output, as schematically shown in Fig. 5. The RF signal input to the drain port of one FET is then sampled by these narrow pulses. Therefore, a sampled phase-detection output is obtained at the FET source and held on the capacitor.

These circuits were simulated using SPICE. Because this SPD does not need the step recovery diode that is used in ordinary SPD's as a pulse generator, it can operate at a low driving power of 0 dBm.

A photograph of the SPD is shown in Fig. 6. The circuit size is only 2.0×1.5 mm^2. It was fabricated with the same monolithic high-yield MESFET process used to fabricate the 30-GHz oscillator chip. This implies that the MMIC SPD can also be integrated into the 30-GHz oscillator chip.

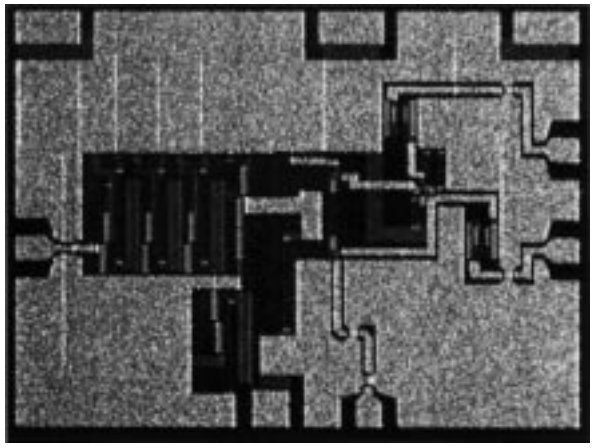


Fig. 6. Photograph of the MMIC SPD. Chip size is 2.0×1.5 mm^2.

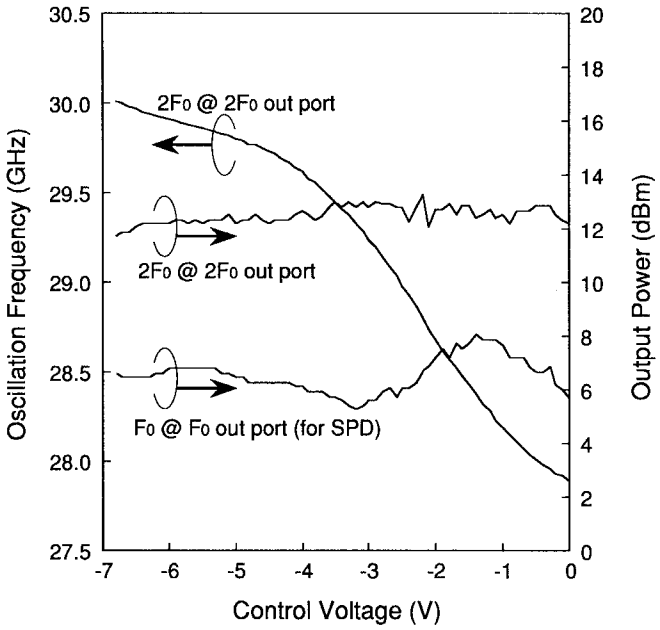


Fig. 7. The tuning characteristic for the 30-GHz oscillator chip.

C. External Components

An analog adder built with a commercially available IC is used for the dc offset of the phase-detection output voltage. No loop filter is applied to control the PLL bandwidth. Instead, a variable resistor after the SPD is used here to optimize it.

IV. Measured Performance

A. Oscillator Free-Running Characteristics

Fig. 7 shows the frequency and output power of the 30-GHz oscillator chip versus tuning voltage across the varactor. Output power of 12.5 dBm $\pm$0.7 dB is obtained throughout the frequency range. A large signal is, therefore, fed into the frequency doubler, which uses harmonics caused by nonlinearity. The fundamental frequency oscillation for the PLL is also shown. Output power of 6.7 dBm $\pm$1.4 dB is supplied to the SPD, which is sufficiently large for the driving power.

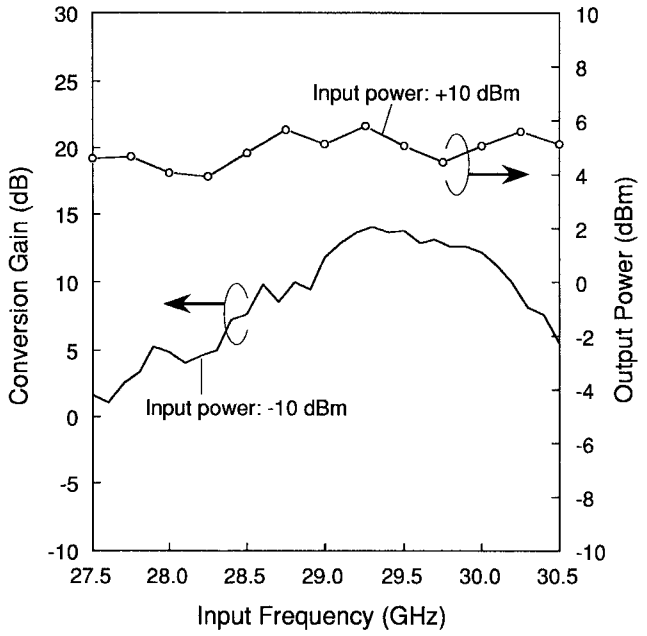


Fig. 8. The conversion gain at low input power and saturated output at high input power for the 30–60-GHz doubler chip.

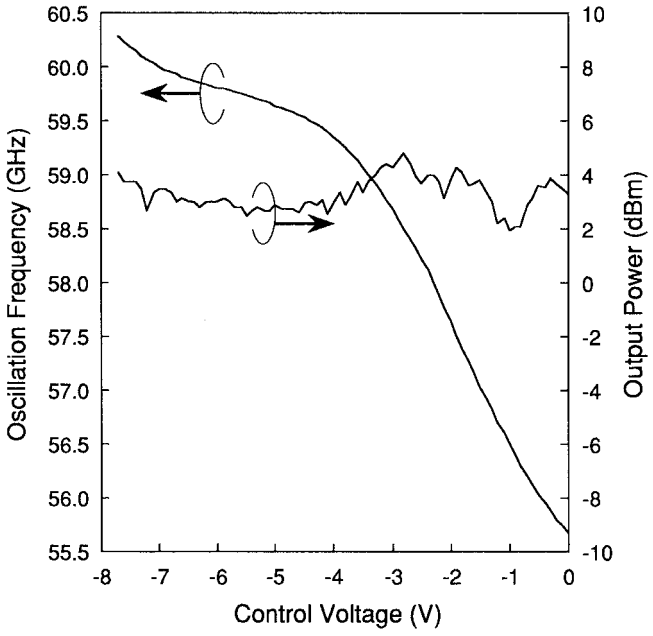


Fig. 9. The tuning characteristic for the oscillator chip set.

The frequency responses of the 30–60-GHz doubler chip at low input power are shown in Fig. 8. The conversion gain is 14 dB with an input frequency of 29.2 GHz. Gain is decreased when the input signal is large. Consequently, a fairly stable output level is achieved over a wide frequency range for a large signal input, as also shown in Fig. 8.

Fig. 9 shows the frequency and output power of the oscillator chip set versus the tuning voltage across the varactor. The frequency can be tuned smoothly from 55.6 to 60.3 GHz as the tuning voltage is changed from 0 to -7.7 V. Output power of 3.5 dBm ± 1.5 dB is obtained throughout the frequency range. This is near the output saturation of a 60-GHz amplifier fabricated with a low-noise PM HEMT, and is sufficient for a LO signal for a millimeter-wave active frequency converter. The single-sideband (SSB) phase noise of free-running oscillation at the V-band was measured with a spectrum analyzer (Fig. 10). It is less than -80 dBc/Hz at 1-MHz offset when the tuning voltage is set to -5 V.

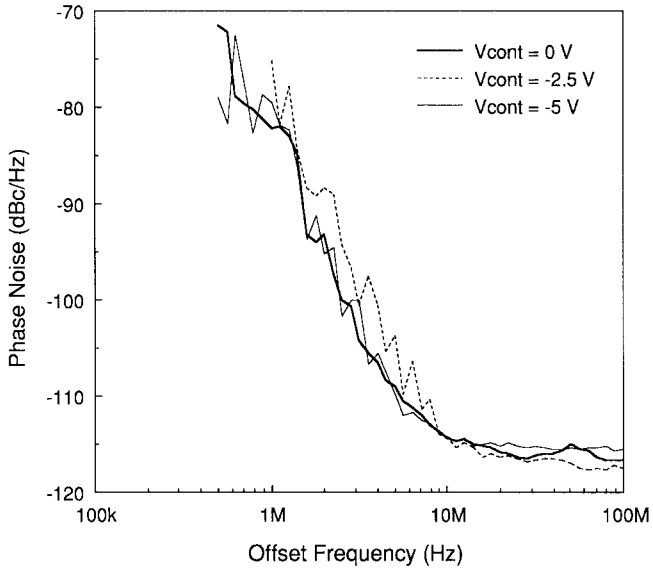


Fig. 10. The SSB phase noise for the oscillator chip set (free-run).

B. SPD and PLO Performance

Fig. 11 shows the measured phase detection output voltage of the SPD versus RF input frequency. An output of more than 100 mV_{pp} above 15 GHz is obtained with a 100-MHz, 0-dBm reference signal.

This SPD was applied to the oscillator. Phase-locking was achieved with 800-MHz steps from 56.0–60.0 GHz when the reference frequency was 200 MHz. An example of the observed phase-locked spectrum at 60.0 GHz is shown in Fig. 12(a). The free-running spectrum near 60 GHz is shown in Fig. 12(b) for comparison. Note that the frequency spans in these two figures are quite different. Fig. 12(c) shows the panoramic wide span PLO spectrum of Fig. 12(a). The two traces in Fig. 12(c) were obtained using two alternating

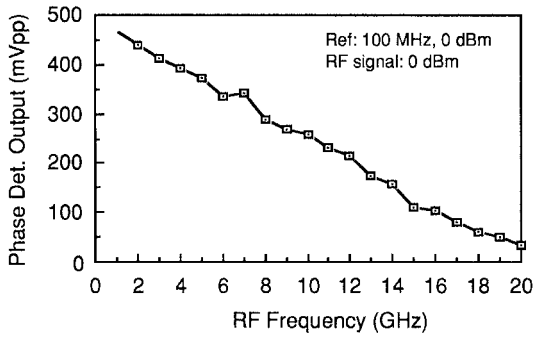
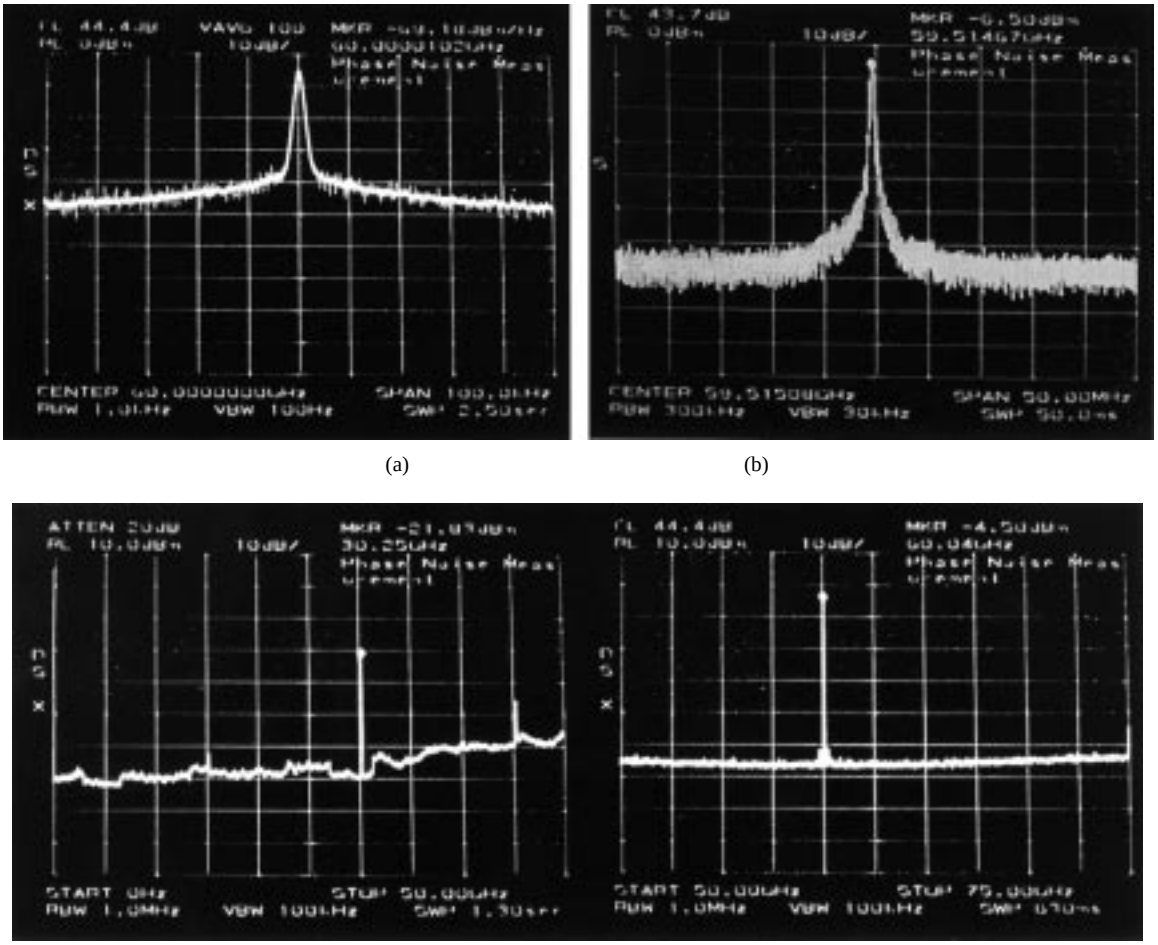


Fig. 11. The output voltage of the MMIC SPD as a function of RF input frequency.

spectrum-analyzer mixer modes. No spurs can be seen except for the fundamental 15.0-GHz signal and harmonic 30.0- and



(a) (b)

(c)

Fig. 12. PLO output spectra. (a) Near a carrier with locked state, H: 10 kHz/div, V: 10 dB/div, RBW: 1 kHz. (b) Near a carrier with free-run ($V_c = -5$ V), H: 5 MHz/div, V: 10 dB/div, RBW: 300 kHz. (c) Panoramic view, H: dc-50 GHz (left), 50–75 GHz (right), V: 10 dB/div, RBW: 1 MHz.

45.0-GHz signals. For V-band use, the loss of the cable between the output terminal and spectrum analyzer is more than 6 dB around 60 GHz, and it is far more than the loss of the cable below the V-band. Thus, these undesired harmonics are actually suppressed further than can be seen in the figure. Because these signals are far from the desired 60-GHz signal, they can be easily eliminated by a simple high-pass filter. The measured SSB phase noise for phase-locked oscillation at 60 GHz is shown in Fig. 13. The phase noise is −64 dBc/Hz at 10-kHz offset from the carrier.

The total power consumption of the PLO is about 2100 mW; 350 mW for the 30-GHz oscillator chip, 60 mW for the 30–60-GHz doubler chip, and 850 mW for the SPD.

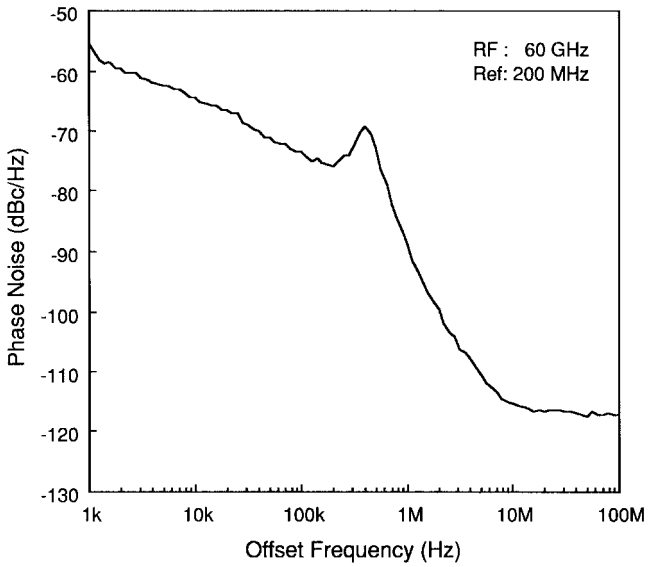


Fig. 13. The SSB phase noise for the V-band SPD PLO.

V. Conclusion

This paper has described a V-band full-monolithic PLO chip set that, to the authors' knowledge, is the most compact one ever developed. The uniplanar structure reduces the circuit size drastically and the use of a GaAs MMIC SPD makes the PLO simple and compact. Consequently, all the circuits can be integrated into as few as three chips, and the chip area is 5.5 mm^2 for the oscillator and 3.0 mm^2 for the SPD. The oscillator stabilized at 56.0–60.0 GHz in a phase-locked condition with a step four times the size of the PLL reference frequency. The SSB phase noise in the loop bandwidth is suppressed to the noise floor of the PLL, and it is as low as −64 dBc/Hz

at 10 kHz offset from 60 GHz in spite of the low Q full-monolithic circuitry. This approach will surely contribute to the development of small and simple V-band MMIC PLO's for communication equipment.

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